

Q1P High-Speed Input/Output Function Test

基本信息说明

产 品 类 型	Q 系列	产 品 型 号	HCQ1P-1300-D4	保密等级	☐ 公开 ☒ 内部分享 ☐ 保密
				文档编号	-
修 订	-	作 者	王跃	发布日期	
本文档使用硬件设备和软件工具					
- Q 系列上位编程软件 HCP Works3 V1.3.0 - 控制器：HCQ1P-1300-D4					
本文档测试目标：验证新产品高速输入输出功能					
文档更新和发布状态：					
发布日期		版本	更新内容		发布状态

Contents

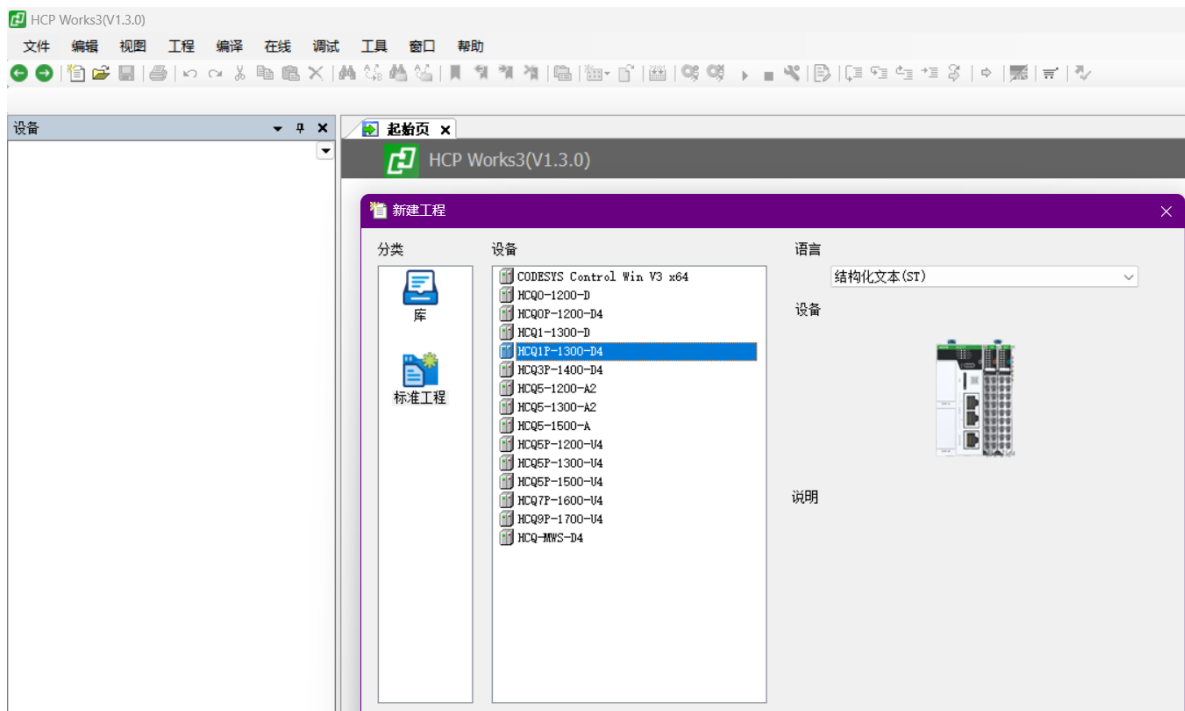
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一、 High-speed input and output functionality

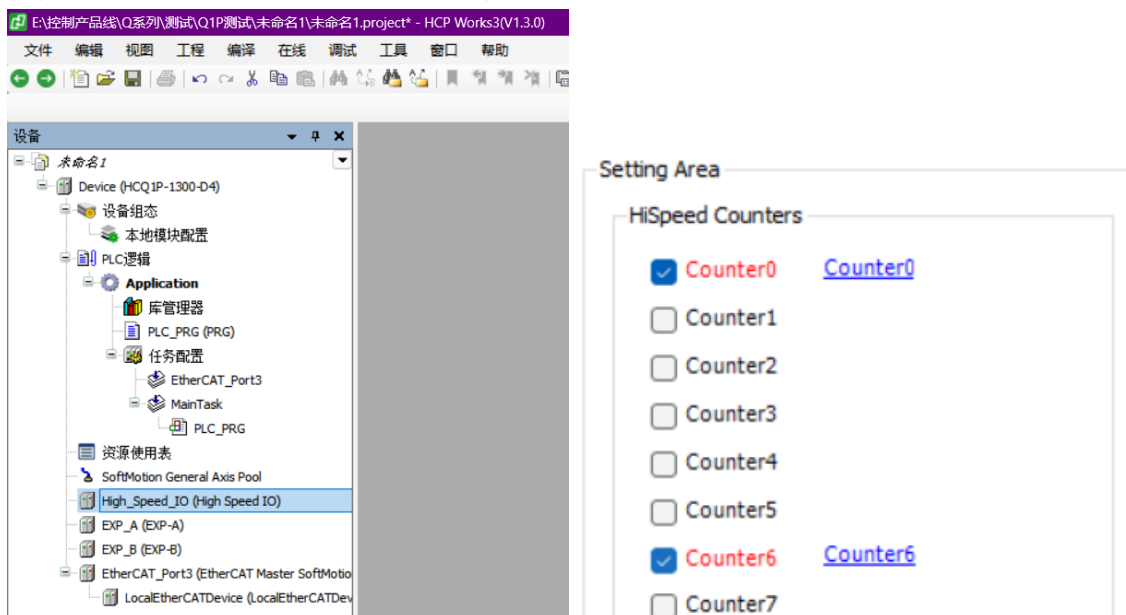
1.1 Q1P High-Speed Counting, Hardware Reset, Probe Latch Function

1.1.1 Configuration Settings

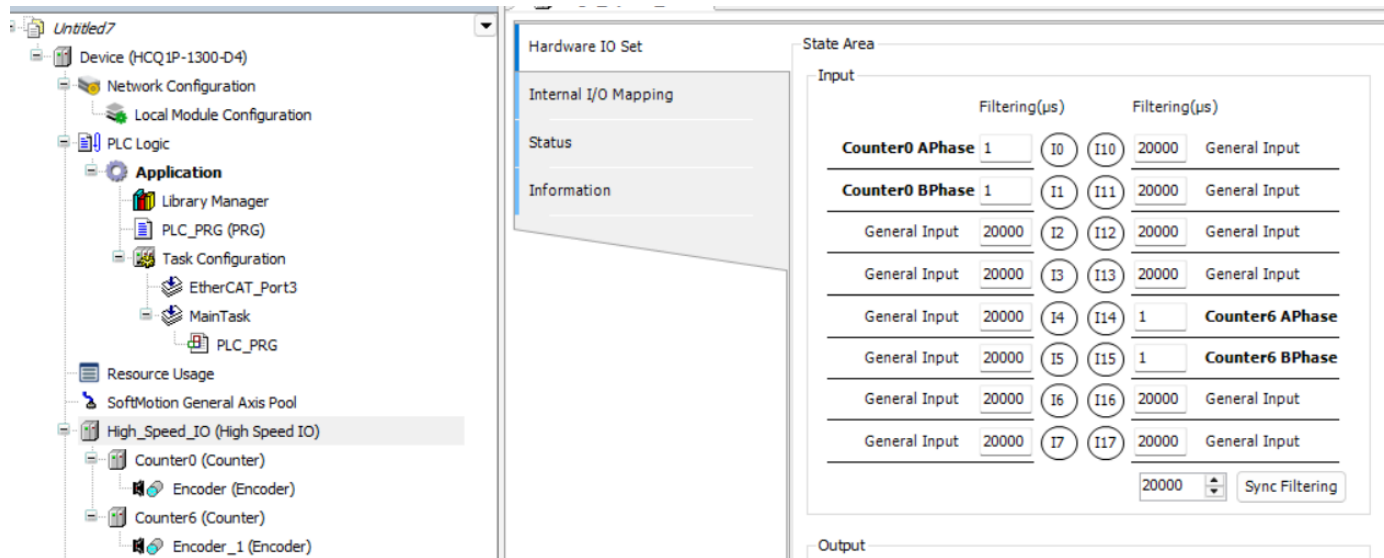
Create new project, select HCQ1P-1300-D4.



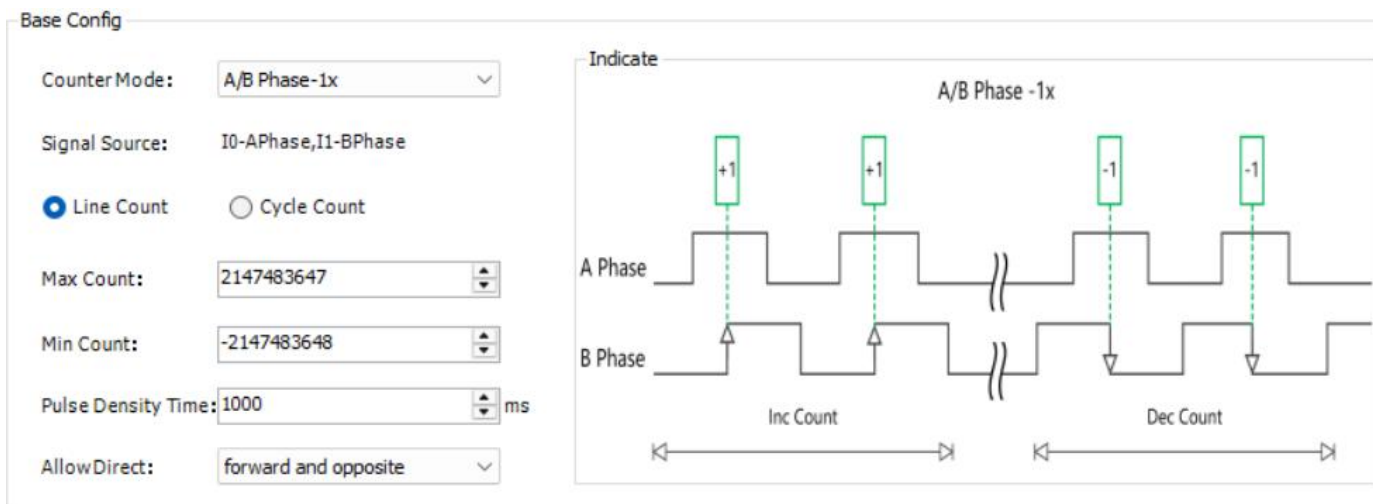
。 Double-click High_Speed_IO in the device to open its tab. In the configuration section, check Counter 0 for high-speed counting. The device tree will then automatically generate an encoder shaft.



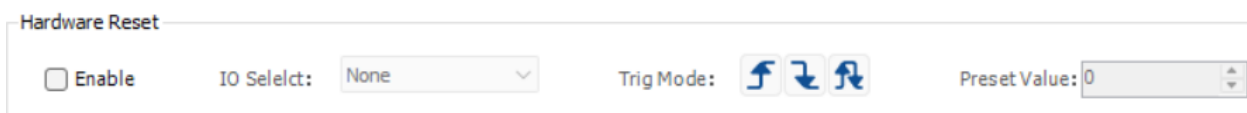
In the input area of the status zone, I0 and I1 will display the connection to phase A and phase B of the encoder, respectively.



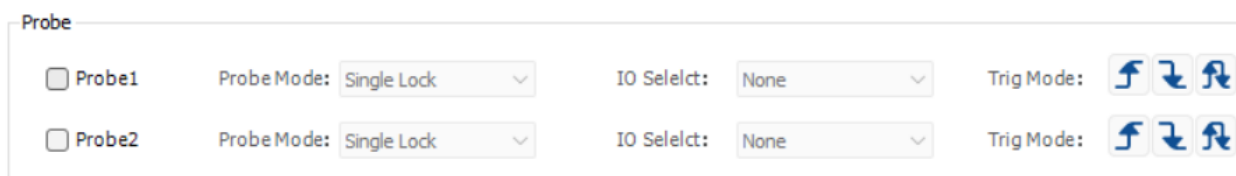
Double-click on Counter0 under High_Speed_IO, and in the tab that appears, you can configure the counter mode (A/B phase 1x, 2x, 4x multiplication, CW/CCW, Pulse + Direction) and other basic settings.



The hardware reset function can also be enabled by selecting a trigger terminal. The trigger modes include rising edge, falling edge, and both rising and falling edges. Triggering the corresponding terminal will modify the current position of the counter to the set preset value.



Each counter has two probes, and each probe can latch the current value of the counter in single or continuous mode. The latching can be set to rising edge, falling edge, or both rising and falling edges.



Double-click on Encoder under Counter0 to configure the encoder axis parameters.

1.1.2 Version Compatibility Description

The device information for the HCQ1P-1300-D4 is as follows:

设备信息

型号和版本

PLC型号:	HCQ1P-1300-D4	设备名称:	HCQ1P-1300-D4
系统版本:	2.1.0	应用版本:	1.00.01.02
FPGA版本:	02020007	显示模块版本:	

获取信息

The IDE version must be HCP Works3 V1.3.0 or higher.

1.1.3 Treset content

Add the **hcfaPlcLib** library in the Library Manager. In the program, call the function blocks **FB_Encoder** and **FB_Latch** from the **HighSpeed_V2** section under **HighSpeed I/O** in the **hcfaPlcLib** library.

The screenshot shows the Library Manager window with the following structure:

- 库管理器
 - 添加库
 - 删除库
 - 属性
 - 详细信息
 - 占位符
 - 库存储
 - 图标图例...
 - Summary...
- 名称

名称	命名空间	有效的版本
3SLicense = 3SLicense, 3.5.17.0 (3S - Smart Software Solutions GmbH)	_3S_LICENSE	3.5.17.0
BreakpointLogging = Breakpoint Logging Functions, 3.5.17.0 (3S - Smart Software Solutions GmbH)	BPLog	3.5.17.0
hcfaPlcLib = hcfaPlcLib, 1.3.3.3 (HCFA)	hcfaPlcLib	1.3.3.3
hcfaPlcLib, 1.3.3.3 (HCFA)	hcfaPlcLib	1.3.3.3
IODrvEtherCAT = IODrvEtherCAT, 3.5.17.0 (3S - Smart Software Solutions GmbH)	IoDrvEthercatLib	3.5.17.0
IoStandard = IoStandard, 3.5.13.0 (System)	IoStandard	3.5.13.0
SM3_Basic = SM3_Basic, 4.10.0.0 (3S - Smart Software Solutions GmbH)	SM3_Basic	4.10.0.0
- hcfaPlcLib, 1.3.3.3 (HCFA)
 - Algorithm
 - Communication
 - DeviceSet
 - HighSpeed I/O
 - HighSpeed_V1
 - HighSpeed_V2
 - Data types
 - Functional block
 - FB_Encoder
 - FB_Latch
 - FB_PresetValue
 - FB_RateMeasure
 - HighSpeed Axis/Encoder
 - PWM
 - Images
 - MutiCoreSet
 - PlcInfoLib
 - ProgramControl

- FB_Encoder (FB)

FUNCTION_BLOCK FB_Encoder

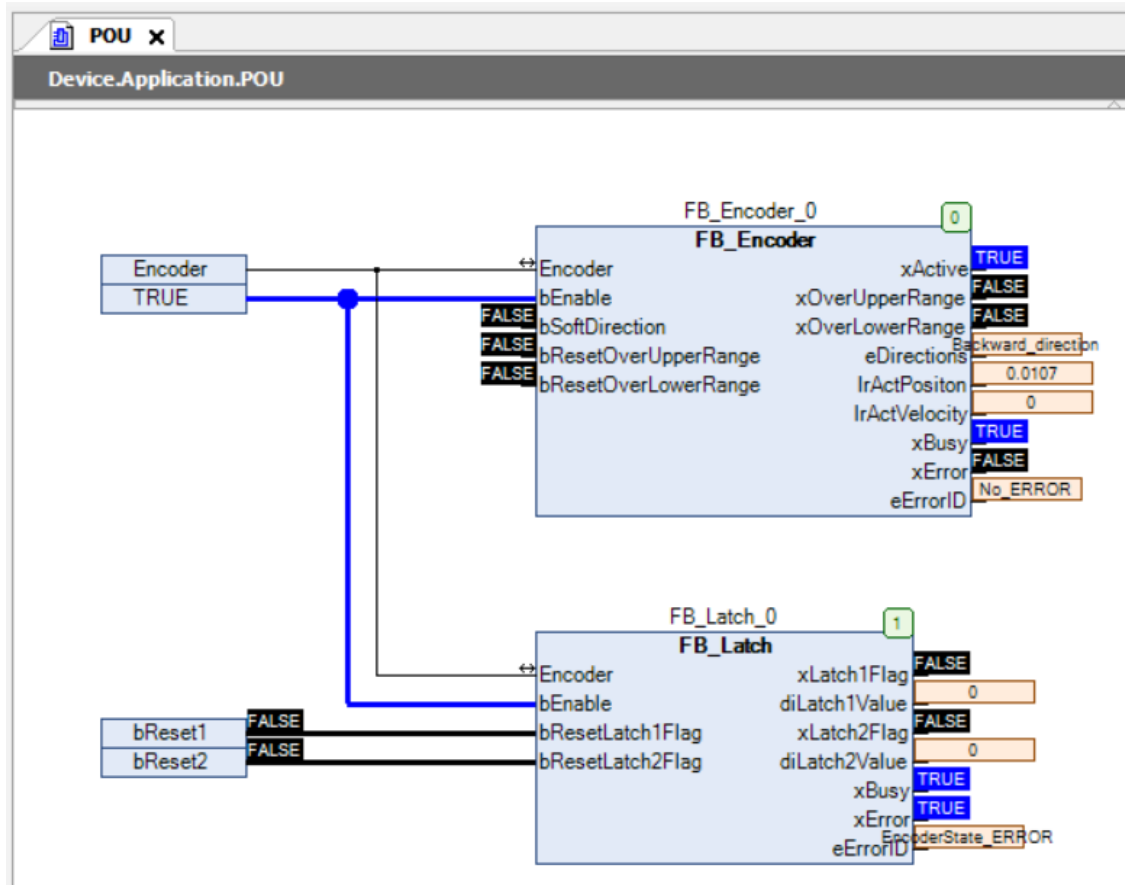
Encoder enable function block

It is used to enable the encoder and Obtain the xActive、IrActVelocity `` of the Encoder.

InOut:

Scope	Name	Type
Inout	Encoder	Encoder_REF_Pulse
Input	bEnable	BOOL
	bSoftDirection	BOOL
	bResetOverUpperRange	BOOL
	bResetOverLowerRange	BOOL

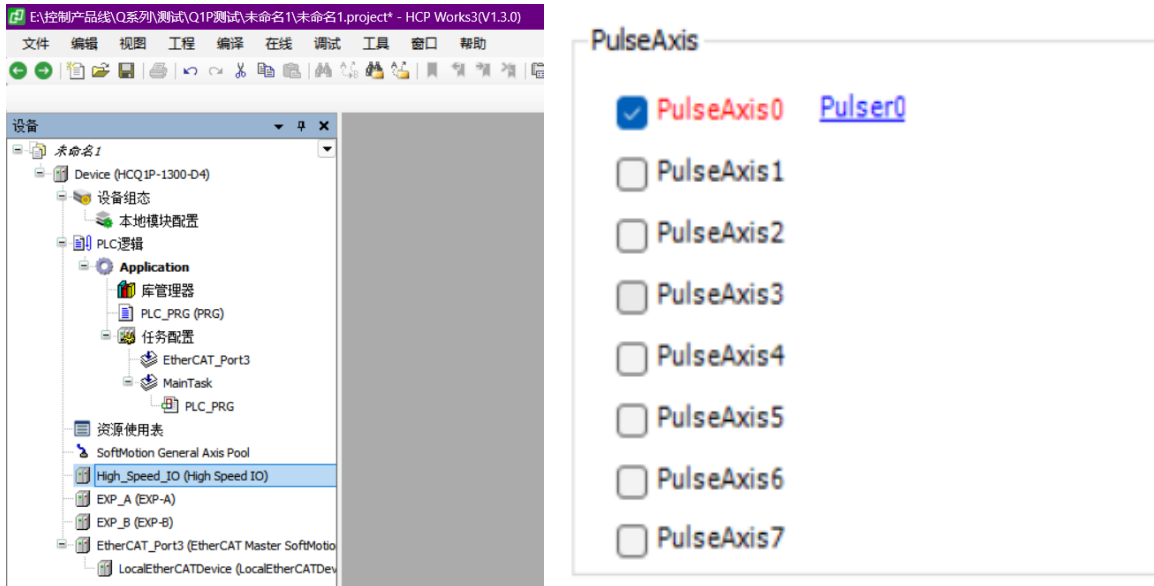
Rotating the encoder will show changes in the **IrActPosition** of FB_Encoder_0. Triggering the signal on terminal I3 will latch the current counter value into **diLatch1Value** of FB_Latch_0. If the encoder shaft continues to rotate and terminal I3 is triggered again, the latched value in diLatch1Value remains unchanged, indicating that this is a single-trigger mode. Latching can only be performed again after bResetLatch1Flag is triggered and the xLatch1Flag is reset. In contrast, terminal I4 can continuously latch the counter value. Triggering terminal I2 will change the current counter value to the preset value.



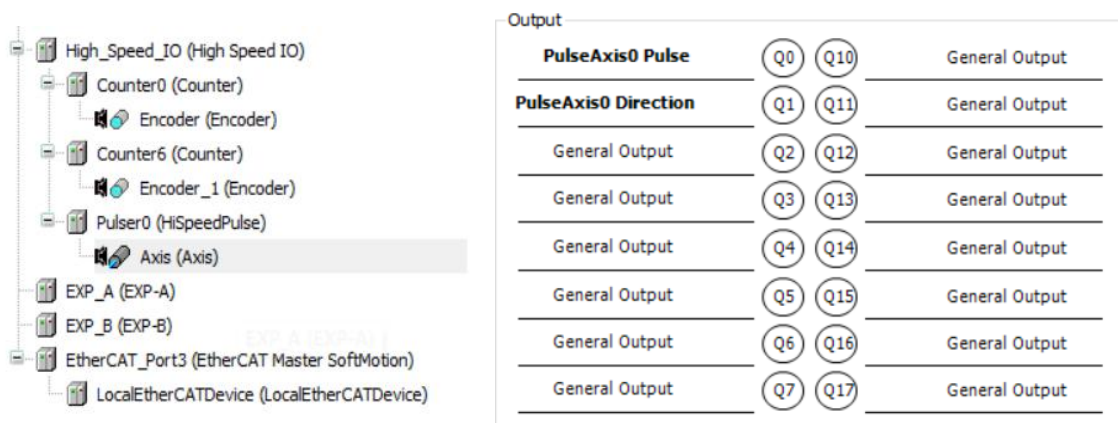
1.2 Q1P High-Speed Output

1.2.1 Configuration Settings

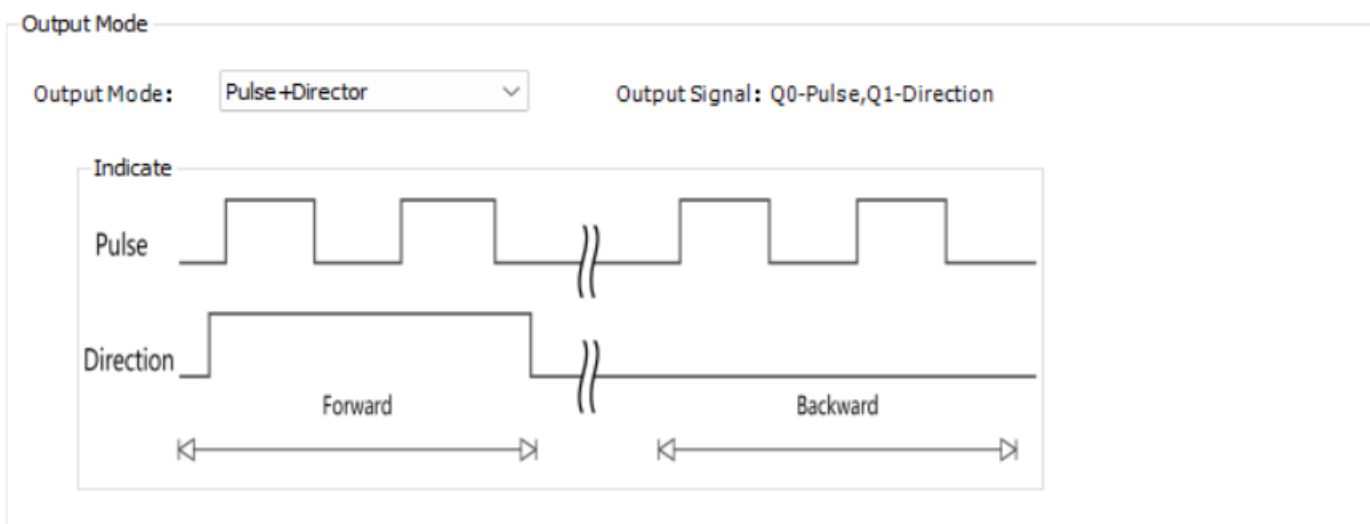
Double-click on High_Speed_IO in the device tree to open the configuration tab. In the configuration area, check the box for Pulse Axis 0, and the pulse axis will be automatically generated in the device tree.



In the output area of the status zone, Q0 and Q1 will display the connection to the pulse and direction of the pulse axis, respectively.



Double-click on Pulser0 under High_Speed_IO. In the tab that opens, you can configure the pulse output mode (A/B phase, CW/CCW, Pulse + Direction).



Double-click on **Axis** under **Pulser0** to configure the axis parameters. It is important to note that the maximum frequency for high-speed output is **200 kHz**. With the default setting of **10,000** pulses per revolution, gear ratio of **1:1**, and a working travel of **1**, the maximum allowable speed setting is **20**.

单位换算公式:

参考

$$\text{脉冲数 (pulse)} = \frac{(1) \text{ 电机旋转一圈的指令脉冲数 [DINT]}}{(2) \text{ 工作台旋转一圈的工作行程 [LREAL]}} \times \frac{(4) \text{ 齿轮比分子 [DINT]}}{(3) \text{ 齿轮比分母 [DINT]}} \times \text{移动距离 [用户单位]}$$

M:电机 W:工作台

电机旋转一圈的指令脉冲数:

(1)

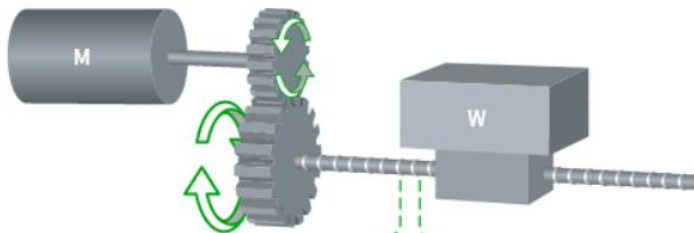
(指令脉冲/转)

齿轮比分子 (齿数): (4)

(3) 齿轮比分母 (齿数):

(2) 工作台旋转一圈的工作行程:

(毫米/转)



1.2.2 Version Compatibility Description

The device information for the HCQ1P-1300-D4 is as follows:

设备信息

型号和版本

PLC型号:	HCQ1P-1300-D4	设备名称:	HCQ1P-1300-D4
系统版本:	2.1.0	应用版本:	1.00.01.02
FPGA版本:	02020007	显示模块版本:	

1.2.3 Treset content

In the new version, the high-speed output axis supports all MC commands except for MC_Home.

